

FIG. 2

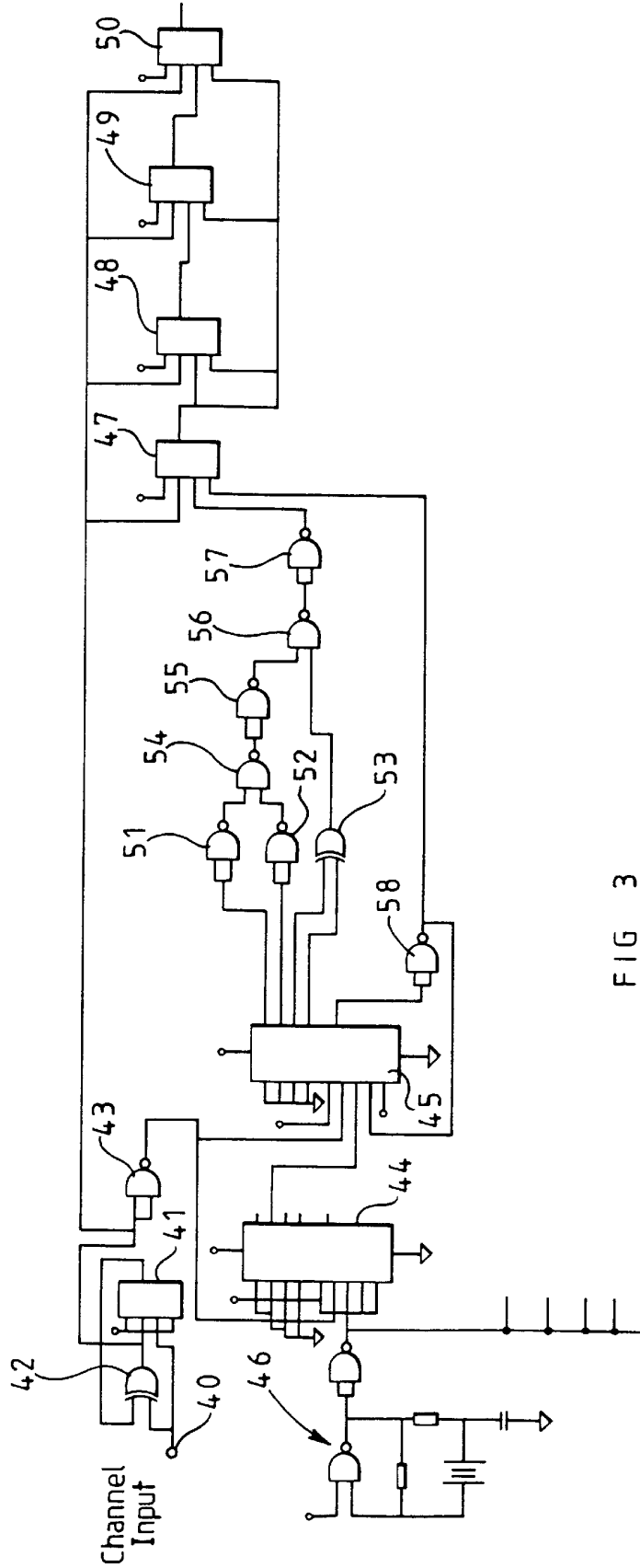


FIG. 3

REPEATER FOR USE IN A CONTROL NETWORK

This is a divisional of application Ser. No. 08/080,717, filed Jun. 24, 1993, now U.S. Pat. No. 5,588,021

BACKGROUND OF THE INVENTION

This invention relates to a repeater for use in a control network. The repeater is of particular utility in a stage lighting control network, but is also usable in other applications.

In a stage lighting control network a branching or tree topology is preferable to a ring or star topology, but noise problems caused by repeated division of control signals flowing outwardly from the main station along the tree to the lamp stations arise and there is also a problem concerning the routing of signals flowing inwardly from the lamp stations to the main console.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a repeater for use in dividing control signals into a plurality of branches whilst avoiding noise problems and also enabling routing of signals from outstations to a main control station.

A repeater in accordance with the invention comprises a root input/output isolating transformer, a plurality of branch input/output isolating transformers, a line receiver circuit and a line driver circuit associated with each of said isolating transformers, common voltage detector means for detecting a common voltage at the root side of said root isolating transformer, common voltage applying means for applying to the branch side of each of the branch isolating transformers a common mode voltage determined by said common voltage detector means, normal data flow enabling means for enabling the line receiver circuit associated with the root isolating transformer and the line driver circuit associated with the branch isolating transformers when a normal common mode voltage is detected, so that data signals received by the root isolating transformer are transmitted from each of the branch isolating transformers, reverse data flow enabling means for enabling the line receivers associated with the branch isolating transformers when a different common mode voltage is detected, a data signal discriminating means for detecting the presence of valid data signals at the output of any one of the line receivers associated with the branch isolating transformers, and means for enabling the line transmitter associated with root isolating transformer when such valid data signals are detected and for routing to it the output of the one of the line receivers at which valid data signals have been detected.

DESCRIPTION OF THE INVENTION

An example of the invention is shown in the accompanying drawings in which FIG. 1 is a schematic diagram of a control network for controlling stage lighting, FIG. 2 is a schematic circuit diagram of a repeater which is used in the network of FIG. 1 and FIG. 3 is the schematic circuit diagram of a signal validity checker included in the circuit of FIG. 2.

DETAILED DESCRIPTION

The network connects a control console 10 to a plurality of lamps 11. The control console 10 has various manually actuable input devices which provide inputs to a micro-computer and displays driven by the micro-computer. There

is an associated hard disk drive which can be used to store sequences of operations, for transmission over the network. The micro-computer includes a serial communication controller based on a Zilog Z8530 integrated circuit set up to operate in FMO mode using the SDLC communication protocols.

Each of the lamps also includes a micro-processor with a Z8530 serial communication controller. The micro-processor receives commands from the network and controls a plurality of individual functions of the lamp, such as azimuth and elevation angles, colour control, gobo selection and rotation and others. Each lamp micro-processor has its program in ROM which also stores data uniquely identifying the lamp and its type.

The network is used mainly for the transmission of commands from the console micro-computer to the micro-processors in the lamps, but there is occasionally a need for data to be transmitted in the opposite direction, for example during set-up, when each lamp is required to inform the console of its unique identification data and its type code. This can be accomplished by having the console micro-computer broadcast a request to all the lamps. The lamp micro-processors respond by transmitting back the requested data after a delay dependent on the identification data. The lamps thus transmit their data in different time slots, enabling the console micro-computer to receive the data over a period.

The communication controllers of the console and the individual lamps each have an isolating transformer providing the path for two-way communication with the network cabling and the console microcomputer can impress a common mode voltage on the cabling to indicate whether it is currently operating in transmit mode or receive mode. A negative voltage relative to ground indicates that the console is transmitting, a positive common mode voltage indicating that it is ready to receive.

The network is configured as a multi-branched tree. The console has outputs connected to the "root" side of up to six repeaters 12 which split transmitted data signals between six branches or selectively routes data from the branches to the root. Each repeater branch can drive up to six lamp units 11 and connections to these are made via truss boxes 13 which simply split the incoming signals into six branches in parallel. The truss boxes 13 are also used in the distribution of electrical power to the lamp units. Where there are six repeaters as shown, six truss boxes per repeater and six lamp units per truss box, a maximum of 216 lamp units can be controlled. If an even larger number of lamp units is required for a particular set-up, additional repeaters can be employed, so that, for example, one or each of the repeaters 12 shown drives six further repeaters each of which drives 36 lamps via six truss boxes. A system employing six first level repeaters and thirty six second level repeaters can support up to 1296 lamp units.

The repeater is shown in more detail in FIG. 2. The repeater includes a root input/output isolating transformer T_1 and six branch input/output isolating transformers of which three T_2 , T_3 and T_4 are shown. The repeater side of transformer T_1 is connected to the inputs of a line receiver 30 (one quarter of an i.c. type 28LS32) and to the balanced outputs of a line driver 31 (one half of an i.c. type 3691). A logic circuit 32 to be described in more detail hereinafter controls an enable input of the line driver 31 and also controls routing of data signals from one of the branch transformers. The receiver 30 also has an enable terminal which is controlled by a common mode voltage detecting circuit.

This common mode voltage detecting circuit includes a pair of resistors R_1, R_2 connected to the cable side of the root transformer T_1 . These resistors R_1 and R_2 are connected together and their common point is connected by a resistor R_3 to the cathode of a diode D_1 , the anode of which is connected to the grounded screening of the network cable. The light emitting diode D_2 of an opto-isolator D_1 is connected across the diode D_1 so that it conducts when the common mode voltage is positive, but is turned off when such voltage is negative. The output of the optoisolator is connected to both inputs of a NAND gate N_1 the output of which is connected to both inputs of a second NAND gate N_2 . The output of gate N_2 is shown connected to a terminal marked **CM5-** and the output of gate N_1 is similarly connected to a terminal marked **CM5+**. The voltage at terminal **CM5-** is high only when the common mode voltage is negative and that at terminal **CM5+** is high whenever the common mode voltage is positive. The enable terminal of the receiver **30** is connected to terminal **CM5+** so that receiver **30** is enabled only when the detected common mode voltage is positive.

Each of the branch isolating transformers T_2, T_3 etc. has an associated line driver and an associated receiver. For this purpose there are three further 3691 integrated circuits and two further 28LS32 integrated circuits. FIG. 2 shows three of the branch isolating transformers which are associated with three receivers sharing a 28LS32 integrated circuit. Two of these transformers are associated with drivers sharing a 3691 integrated circuit. The other three transformers, the other 28LS32ic and the other two 3691 integrated circuits are not shown. Three output terminals (labelled X, Y & Z) of the 28LS32 i.c. are connected to inputs of the logic circuit **32**. The two data inputs (pins 2 and 7) of the 3691 ic are connected to the output of receiver **30**. The transmit enable terminals (pins 3 and 6) of the 3691 i.c. are connected to a terminal labelled Q of the gate array.

The common mode voltage at the branch side of the branch isolating transformers is connected to a drive circuit **33** which applies the common mode voltage to the transformer branch sides by parallel resistors R_{11} to R_{22} .

The logic circuit **32** is a field programmable gate array which is programmed so as normally to enable the line drivers, which are connected to the branch isolating transformers. The **CM5-** signal is normally low and disables the corresponding line receivers. When the **CM5-** signal goes high, indicating that the console is expecting reply signals from the lamps, receiver **30** is disabled and the receivers connected to the branch isolating transformers are enabled by the **CM5-** signal. The gate array **32** disables the drivers associated with the branch side transformers.

The gate array **32** now receives any output provided by all the receivers associated with the branch isolating transformers and tests each signal for valid data signals. Validation is carried out by the circuit shown in FIG. 3 by comparing the time between transitions in the data signals. As the data signals are FMO encoded, they contain a transition at the beginning of each bit cell with either an additional transition at the centre of a bit cell for a "zero" data bit or no centre transition for a "one" data bit. Thus the time between transitions in a valid data signal has one of only two values.

The circuit shown in FIG. 3 is one of six signal validity checkers (forming part of the gate array **32**) which receive signals from the six line receivers and respectively seek to recognise valid data in such signals. The channel input signal is received at a terminal **40** and applied to a D-type flip-flop **41** and to one input of an exclusive OR gate **42**

providing a clock input to the flip-flop. The other input of the exclusive OR gate **42** is connected to the Q output of the flip-flop, so that each transition (from high to low or from low to high) in the input signal is converted by the combination of the exclusive OR gate and the flip-flop to a short duration pulse. This pulse is applied to an NAND gate **43** connected as an inverter. The output of the NAND gate **43** is connected to the reset terminals of two 4-bit counters **44** and **45** which are cascaded to form a counter counting clock pulses from a clock generator running at a frequency which is a multiple of the FMO base frequency.

The pulse from the gate **42** is also supplied to the clock inputs of four flip-flops **47** to **50** which are cascaded to form a shift register. The state of the flip flop **47** is determined by the count state of the counter **45** when the gate **42** emits its pulse on detecting a transition. An array of various gates connected to the data outputs of the counter **45** are connected to control the flip-flop **47** so that its output goes high only when the count held at the transition instant represents the duration of a whole or half FMO cell. At each successive transition, the previous state of each of the flip flops **47** to **50** is passed to the next, but all of the flip-flops **47** to **50** are reset via gate **58** otherwise.

The output of the flip-flop **50** thus goes high only when three successive valid transitions have occurred. When the output of the flip-flop **50** is high, transmission from the associated receiver to the line driver **31** is enabled.

Checking of the validity of the signals on that channel continues, so that the channel can be closed as soon as an invalid transition time is detected. All of the other channels are closed, with no data validity checks being made as long as the signals on the selected channel remain valid.

Since the repeater does not start transmitting signals backwardly until three valid intervals have been detected on the currently active channel, it is necessary to include some irrelevant data signals in the data stream transmitted by each lamp before the SDLC opening flag is transmitted. These can consist of one or more SDLC "abort" sequences (i.e. seven or more "ones"), the number required depending on the number of levels of branching in the tree structure (i.e. the maximum number of repeaters the signals may have to pass through).

With the arrangement described, noise signals from all of the inactive lamp processors are not transmitted back from the repeater. Only a channel which is carrying valid data signals is enabled at any time. As the lamp processors transmit data in different time slots, the closing of all channels once a valid data channel has been detected will not give rise to any lost data. Data from each of the lamps is transmitted along a different path through the network and all the repeaters in that path recognise the valid data and allow it alone to pass. If, by some mischance, there are overlapping transmissions from two lamps units on the same truss box, the signals received on the appropriate channel of the repeater will not meet the validity test and will not be passed forward.

We claim:

1. A communication system comprising:

an input node adapted for communication with a controller and an output node adapted for communication with an object of control, said input node having at least two input lines and including means for receiving a coded communication in a common mode coding scheme which is independent of a common mode voltage on two of said input lines;

a common mode voltage detection circuit, for detecting a polarity of voltage on the common mode input node; and

5

means, responsive to said common mode voltage detection circuit, for controlling a direction of communication such that said communication is in a transmitting mode, which transmits from said input node to said output node when the common mode voltage is a first value, and communication is in a receiving mode, which transmits between said output node and said input node when said common mode voltage is a second value.

2. A system as in claim 1 wherein said first value is any positive voltage and said second value is any negative voltage.

3. A system as in claim 2 wherein said output node further comprises means for detecting a validity of a coded information received from said object of control and enabling a communication only when a valid communication is detected.

4. A communication system, comprising:
an input node, including two lines, said two lines adapted to carry a differential voltage;

6

a first element for determining a sense of said differential voltage between a first sense where a first of said two lines is higher than a second of said two lines, and a second sense where said second of said two lines is higher than said first of said two lines, and producing an output signal indicative of which sense is detected; and

bidirectional communication circuitry, which operates in a first mode to send information in a first direction and which operates in a second mode to send information in a second direction different than said first direction, said bidirectional communication circuitry being responsive to said output signal from said first element, to operate in said first mode when said output signal is in a first state, and to operate in said second mode when said output signal is in said second state.

* * * * *